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Backside FIB/SEM analysis strategy to identify a new failure mode at an automotive magnetic sensor device

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Integrated circuits (IC) used in automotive applications must be produced under high quality standards. To achieve this goal each single fail from qualification or also field application must be traced down to its physical failure root cause to increase the overall device reliability. In most cases the failure analysis (FA) strategy of IC related defects is straight forward by electrical testing, followed by defect localization and finally destructive physical analysis to identify the defect structure and derive the root cause of the electrical malfunction.

In some cases, such a strategy is not straight forward, especially if the failure site can not be exactly located or if the IC-package interaction causes the failure mode.

In this work we will demonstrate a failure root cause analysis of an automotive magnetic field sensor IC which fails by an electrical short between 2 metal layers, fig. 1. Over time a conductive path is created and at a certain resistance the devices fail with increased power consumption. This could be shown several times, but the question stays unanswered over a longer time regarding the primarily root cause. There are different hypotheses discussed, for example electrostatic discharge, package issues as well as imprints induced by probe tools.

In a standard FA procedure, the package is fully removed above the IC to get access to its functional surface structure. Then further localization and preparation steps are following. At this specific case the original root cause could not be identified from frontside, that's why it was decided to turn the preparation starting from backside without removing the package at the frontside. The real challenge was that the failing position could not be localized in detail. Due to the electrical behavior of the sensor and the experiences collected by many fails before the position could be estimated and correlated to a several 10µm long metal network.

To get access to the ROI the Si substrate was mechanically thinned down to around 30µm thickness. After this the remaining silicon was removed by Xe-Plasma FIB trenching down to the active IC structure, fig. 2. Then the metal network was cut

by Ga-FIB at several positions and investigated by passive voltage contrast to identify the shorted part, fig. 3. Finally, the remaining shorted metal lines were screened by forwarding FIB cross sectioning under SEM observation till irregularities (delamination, cracks) could be found in the IC structure. The defect origin could be identified due to the preserved mould compound on top of the IC. A large filler particle touches the IC passivation at the position of the cracks. Due to the mechanical stress during the moulding process these cracks were initiated, later metal was migrating into these cracks forming an electrically conductive path between metal 1 and 2, fig. 4. The same failure mode could be verified at several sensor devices.

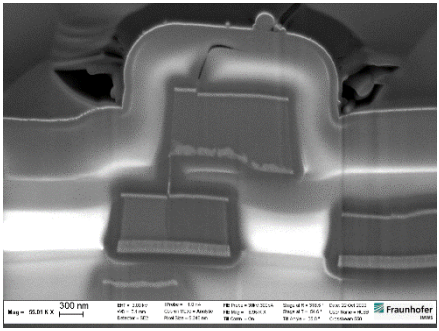

Fig. 1: SEM image of a FIB cross-section showing shorted metal lines due to a metal filled crack in-between these lines

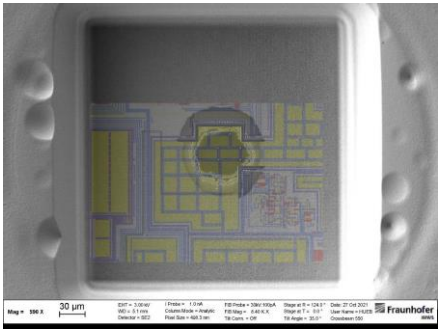

Fig. 2: P-FIB backside trenching of the Si substrate overlaid with the IC layout of the ROI, before and after detailed Ga-FIB investigation

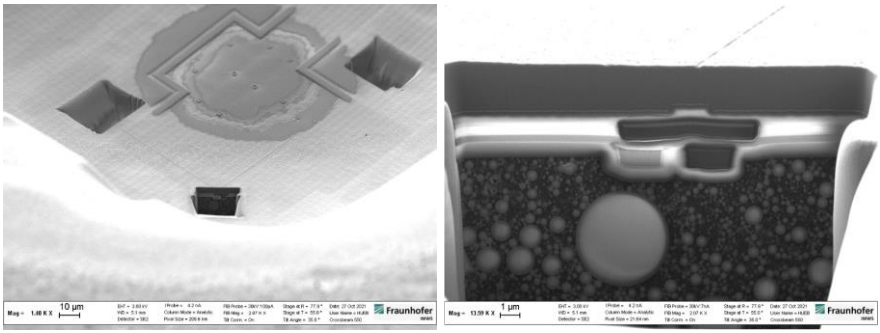

Fig.3: Passive voltage contrast investigation to isolate the defect position in the IC network

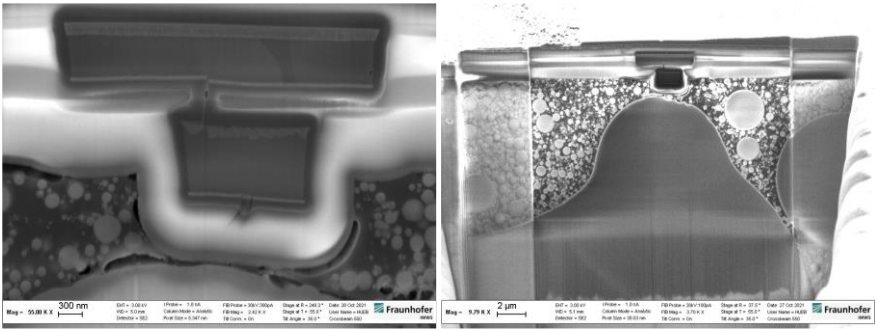

Fig.4: SEM cross-section showing a delaminated mould-passivation interface with cracked chip passivation and interlayer induced by a large filler particle