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Fault Localization in FIB/SEM – combining delayering and EBAC into a cohesive workflow

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Fault localization and fault isolation are important, recurring tasks in many Fault Analysis laboratories. The workflow involves various techniques for deprocessing and delayering the sample including CNC milling, various polishing methods, and lately, with the advent of smaller and smaller technology nodes, PFIB delayering. The latter method yields precise control over the number of layers removed while allowing the operator to open large windows into the sample.

Once the target layer is exposed, electrical testing methods such as EBIC (Electron Beam Induced Current) or EBAC (Electron Beam Absorbed Current) as well as nanoprobe experiments for transistor characterization can be performed. Depending on the obtained results, further delayering may be required. Or, if the fault is located, a TEM slice may be prepared in order to further elucidate the fault's root cause.

Thus, it is advantageous to combine the electrical characterization measurement and the PFIB delayering into a single tool – thereby circumventing the need to move the sample back and forth between tools. This minimizes the sample's exposure to air (which minimizes contamination on the sample) and significantly speeds up the time to result. The images in Fig. 1 and Fig. 2 show the proposed setup as well as a micrograph of a typical sample with probes in place for EBAC analysis.

In this work, the proposed tool configuration for performing the combined workflow described above will be presented.

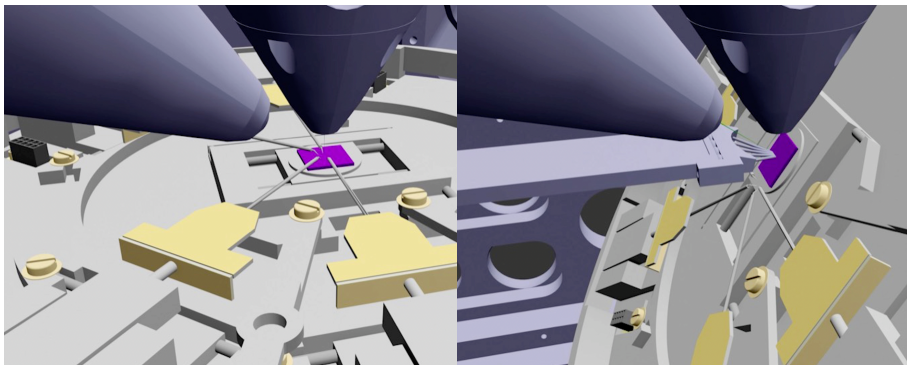


Fig. 1: EBAC configuration (left) and delayering configuration (right) with the stage tilted to FIB angle and the GIS inserted. Note that the sample was shifted using the integrated substage such that the distance between the probe tips and the FIB is maximized in order prevent contamination of the probe tips.

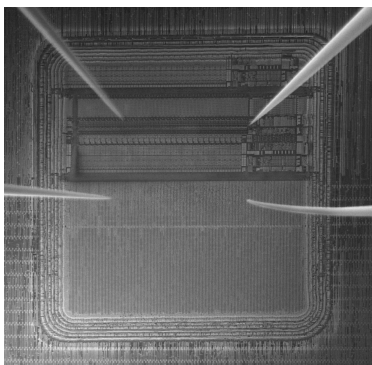


Fig. 2: Four probe tips placed in close vicinity to the sample in preparation for an EBAC analysis (courtesy AMD Singapore)